UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

SOUTHERN DIVISION

LIMESTONE MEMORY SYSTEMS LLC, a California Limited Liability Company, **Plaintiff,** **vs.** **MICRON TECHNOLOGY, INC., et al,** **Defendants.**	**Case No.:** 8:15-cv-00278-DOC (KESx) 8:15-cv-00648-DOC (KESx) 8:15-cv-00650-DOC (KESx) 8:15-cv-00652-DOC (KESx) 8:15-cv-00653-DOC (KESx) 8:15-cv-00654-DOC (KESx) 8:15-cv-00658-DOC (KESx) **CLAIMS CONSTRUCTION ORDER**

I. INTRODUCTION

In this action, plaintiff Limestone Memory Systems, LLC ("Limestone") accuses Defendants of infringing three patents, each related to dynamic random-access memory ("DRAM") technologies. Specifically, Limestone asserts claims 1 and 2 of U.S. Patent No. 5,805,504 ("the '504 Patent"), claim 3 of U.S. Patent No. 6,233,181 ("the '181 Patent"), and claims 13–14 of U.S. Patent No. 6,697,296 ("the '296 Patent"). Defendants have denied infringement and asserted various defenses, including that several of the asserted claims are invalid, because the claims language is indefinite.

II. LEGAL STANDARDS FOR CLAIM CONSTRUCTION

A. Terms Must Be Construed as Understood Within the Field of the Invention

Claims construction consists of determining the meaning of the sometimes terse or unfamiliar words used in patent claims. *Gart v. Logitech, Inc.,* 254 F.3d 1334, 1339 (Fed. Cir. 2001). Claim construction is a matter of law for the Court. *Markman v. Westview Instr., Inc.*, 52 F.3d 967, 977 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). "When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it." *O2 Micro Intern. Ltd. v. Beyond Innovation Tech. Co.*, 521 F. 3d 1351, 1362 (Fed. Cir. 2008).

As the Federal Circuit has observed, claims construction must begin from the proper starting point:

> Th[e] starting point is … the well-settled understanding that inventors are typically persons skilled in the field of the invention and that *patents are* addressed to and *intended to be read by others of skill in the pertinent art*. See *Verve, LLC v. Crane Cams, Inc.*, 311 F.3d 1116, 1119 (Fed.Cir.2002) (patent documents are meant to be "a concise statement for persons in the field").

Phillips v. AWH Corp., 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc) (emphasis added). In other words, "[t]he descriptions in patents are not addressed to the public generally, to lawyers or to judges, but, as section 112 says, to those skilled in the art to which the invention pertains or with which it is most nearly connected." *Id.*, quoting *In re Nelson*, 47 C.C.P.A. 1031, 280 F.2d 172, 181 (1960).

Courts therefore strive to understand claim terms according to their ordinary and customary meaning *as used in the field of invention*. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The focus is on "what one of ordinary skill in the art at the time of the invention would have understood the term to mean." *Markman*, 52 F.3d at 986. A person of ordinary skill in the art (or "POSITA") is "deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips*, 415 F.3d at 1313. The parties offer similar descriptions of the level of skill in the art for each of the patents-in-suit. (Khatri Decl. ¶ 20–25; Rhyne Decl. ¶ 18–22; Pedram Inv. Rep ¶¶ 56–57.) Further, the parties have stipulated to the appointment of a Special Technical Master, Dr. Nader Bagherzadeh, to assist the Court in determining how a POSITA would understand the technical terms in the disputed claim language.

"In some cases, the ordinary meaning of claim language ... may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Id.* at 1314. For instance, terms such as "above, "below," "surrounding," etc. are not technical terms requiring any particular skill in the subject field. Likewise, the meaning of some terms of degree ("close," "approximately," "substantial") are often readily apparent from the context of the surrounding claim language and may be deemed unambiguous so as to render analysis or interpretation to be unnecessary. *Genes Industry, Inc. v. Advanced Components Specialist, Inc.* 2005 WL 6287758 at *3 (C.D. Cal. June 22, 2005) (concluding that "[t]he term 'at least' does not need to be construed differently than its ordinary, common usage").

Here, there are several instances in which one of the parties asserts that a disputed claim terms is unambiguous and requires no construction, while the other party argues that the term has a specialized meaning. In such cases, the initial step in the Court's analysis is to determine whether construction of the language is necessary in the first place.

B. Sources for Deriving Claim Meaning

1. Intrinsic Evidence

Once it is determined that claim language must be construed, the court looks to three primary sources: the claims, the specification, and the prosecution history. Collectively, these are often referred to as "intrinsic evidence." *Markman*, 52 F.3d at 979.

The Federal Circuit has emphasized that "the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips*, 415 F.3d at 1312 *quoting Innova/Pure* Water*, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). As the claims define the invention, the claim language is the most important source for a court to consider in construing the claim terms. *Phillips*, 415 F.3d at 1312. The second most critical source of intrinsic evidence is the patent specification, which "contain[s] a written description of the invention and of the manner and process of making and using it ...." 35 U.S.C. § 112 ¶ 1 (2006). The "specification 'is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Phillips*, 415 F.3d at 1315 quoting *Vitronics*, 90 F.3d at 1582. The third source of intrinsic evidence is the prosecution history, which consists of "the complete record of the proceedings before the Patent Office and includes the prior art cited during examination of the patent." *Id.*, at 1317. The prosecution history is less useful in claim construction, however, because it can itself be ambiguous as it represents ongoing negotiations between the patent applicant and the Patent Office. *Id*.; see *Inverness Med. Switz. GmbH v. Warner Lambert Co*., 309 F.3d 1373, 1380- 82 (Fed. Cir. 2002).

In most situations, an analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term. In such circumstances, it is improper to rely on other

types of evidence, such as expert declarations, treatises, and prior art (collectively, "extrinsic evidence").

2. Extrinsic Evidence

After consideration of the intrinsic evidence, if a court still finds the claim term to be ambiguous, it can look to extrinsic evidence which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Markman*, 52 F.3d at 980. However, such external evidence is "less significant than the intrinsic record in determining the 'legally operative meaning of claim language.'" *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004) quoting *Vanderlande Indus. Nederland BV v. Int'l Trade Comm'n*, 366 F.3d 1311, 1318 (Fed. Cir. 2004).

Here, the parties have submitted extensive extrinsic evidence, including declarations by plaintiff's experts, Dr. V. Thomas Rhyne ("Rhyne Decl.") and Dr. Sunil P. Khatri ("Khatri Decl.") and declarations by Micron's expert Massoud Pedram ("Pedram Decl."). Expert testimony can aid the Court in several ways. It can provide background on the technology, explain how an invention works, ensure that the Court's understanding of the technical aspects of a patent is consistent with those of ordinary skill in the art, and establish the accepted meaning of a claim term in the pertinent field. *Phillips*, 415 F.3d at 1318. However, a court should only consider such testimony in the context of the intrinsic evidence, and may not use it to arrive at a claim construction that contradicts the construction mandated by the intrinsic evidence. *Vitronics,* 90 F.3d at 1583-84. "Indeed, where the patent documents are unambiguous, expert testimony regarding the meaning of a claim is entitled to *no weight*." *Id.*, at 1584 (emphasis added).

Lastly, "a court in its discretion may admit and rely on prior art proffered by one of the parties, whether or not cited in the specification or the file history. This prior art can often help to demonstrate how a disputed term is used by those skilled in the art." *Id*. However, as with other types of extrinsic evidence, reliance on prior art is unnecessary,

and indeed improper, when the disputed terms can be understood from a careful reading of the claims and specifications. *Id.*

C. Defining a Claim by Describing "Means-Plus-Function"

One method an inventor may use in describing the scope of his or her patent is to describe what it does, without specifically reciting the precise mechanism used. Under this approach, the inventor does not describe the physical structure of a particular element in a patented invention, but instead provides only a description of the function performed. 35 U.S.C. §112 ¶ 6 ("Section 112"). ("An element in a claim for a combination may be expressed as a means or step for performing a specified function *without the recital of structure*, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof") (emphasis added).

Structure disclosed in the specification is "corresponding" structure within the meaning of Section 112 only if "the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *B. Braun Medical Inc. v. Abbott Labs et al*., 124 F.3d 1419, 1424 (Fed. Cir. 1997). When the specification indicates that a particular structure performs a claimed function, it is error to include other structures that are unnecessary to perform the claimed function even if those structures directly interact with or are tied to the structure that performs the claimed function. *Northrup Grumman Corp. v. Intel Corp.*, 325 F.3d 1346, 1352 (Fed. Cir. 2003) (finding district court erred by including signals that were to monitored by or generated by the corresponding structure of a means limitation.).

"The question whether a claim element triggers section 112(6) is ordinarily not a difficult one. Claim drafters conventionally use the preface 'means for' (or 'step for') when they intend to invoke section 112(6), and there is therefore seldom any confusion about whether section 112(6) applies to a particular element. *Greenberg v. Ethicon Endo-Surgery, Inc*., 91 F.3d 1580, 1583.

Here, two of the claims in the '504 Patent use the "means for" construction and the parties agree that the claims language must therefore be interpreted in accordance with Section 112. Additionally, Micron contends that a portion of Claim 13 in the '296 Patent triggers the means-plus-function limitation, even though it does not contain the phrases "means for" or "step for," but instead refers to an "activation control circuit." In response, Limestone contends that, as a matter of law, use of the word "circuit" connotes sufficient structure to avoid the application of Section 112.

D. Claim Indefiniteness

In several instances, Micron contends that the subject claim language is indefinite, and therefore violates the basic requirement that a patent must "conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor … regards as the invention." 35 U.S.C. § 112(b).

The definiteness requirement represents "a delicate balance." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 909 (2014). The law "must allow for a modicum of uncertainty" to provide incentives for innovation, but must also require "clear notice of what is claimed, thereby appris[ing] the public of what is still open to them." *Id.*, at 909. What the statute requires "is that a patent's claims, viewed in light of the specification and prosecution history, inform *those skilled in the art* about the scope of the invention with reasonable certainty." *Id.* at 910 (emphasis added). As the Supreme Court has emphasized, in determining whether particular claim language is sufficiently definite, "[o]ne must bear in mind … that patents are "not addressed to lawyers, or even to the public generally," but rather to those skilled in the relevant art. *Id.* at 910. Because definiteness is evaluated from the perspective of one skilled in the relevant art, courts may find expert opinion particularly instructive. *Id.* at 2011 citing *Markman*, 517 U.S. at 389 ("claim construction calls for 'the necessarily sophisticated analysis of the whole document,' and may turn on evaluations of expert testimony").

As with any other invalidity defense, a defendant asserting indefiniteness must prove that defense by clear and convincing evidence. *Microsoft Corp. v. i4i Limited*

Partnership, 564 U.S. 91, 95 (2011); *Dow Chem. Co. v. Nova Chemicals Corp. (Canada)*, 809 F.3d 1223, 1227 (Fed. Cir. 2015.

III. THE PROPER CONSTRUCTION OF THE DISPUTED CLAIM TERMS

On August 9, 2019, the Parties filed Joint Claim Construction Statements (Dkt. Nos. 233-14 and 233-15). Each of these Statements contains a chart setting forth the relevant language of the claim, the proposed construction of that language, and the evidence the party claims to support its proposed construction. Having considered the Statements and the parties' respective briefs and supporting evidence, having heard oral argument, and having conferred with the STM, the Court now construes the relevant claims language as set forth below.

A. The '504 Patent

The '504 patent relates to a "semiconductor memory . . . having a burst mode transfer function." ('504 Patent, 1:9-11). To engage in such a "burst mode transfer," a serial stream of data (i.e., data in a sequential stream) to be written to the DRAM is converted into parallel data (i.e., side-by-side data) so that it can be "simultaneously processed in the inside of the memory." (*Id.*, 1:59-2:3). Limestone accuses Defendants of infringing claims 1-2 of the '504 Patent.

1. Claim 1: "said receiving serial data"

Limestone's Construction	Defendants' Construction
Not indefinite and should be construed as "said received serial data"[1]	Indefinite

Claim 1 recites in part "an input buffer circuit receiving an external data signals continuously and sequentially in time in synchronism with a reference clock signal for converting said receiving_serial data into a parallel data under control of an external command signal and an external address signal …." ('504 patent at 16:64–17:3).

[1] In a March 6, 2019, email, Limestone clarified a clerical error in its proposed construction for this term.

Defendants argue that "said receiving serial data" is indefinite for several reasons. First, Defendants assert that "said receiving serial data" lacks a strict antecedent. For its part, Limestone contends that a POSITA would understand "serial data" in the phrase "said receiving serial data" to refer to the "external data signals" that the input buffer circuit receives "continuously and sequentially." Defendants respond that, when the claims refer back to the "external data signals," they use the phrase "said external data signals." ('504 patent at 17:6; 17:20-18:1). According to Defendants, the use of different terms in a claim requires that the terms be accorded different meanings.

The Court is not convinced that the rigid approach urged by Defendants is consistent with the approach a POSITA would apply, particularly since Defendants' approach renders the claim unintelligible. *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc*., 381 F.3d 1111, 1119-1120 (Fed.Cir. 2004) (refusing to accord different meanings to slightly different terms where doing so would not provide a viable alternative construction of the claims language and stating "we must conclude that this is simply a case where the patentee used different words to express similar concepts, even though it may be confusing drafting practice").

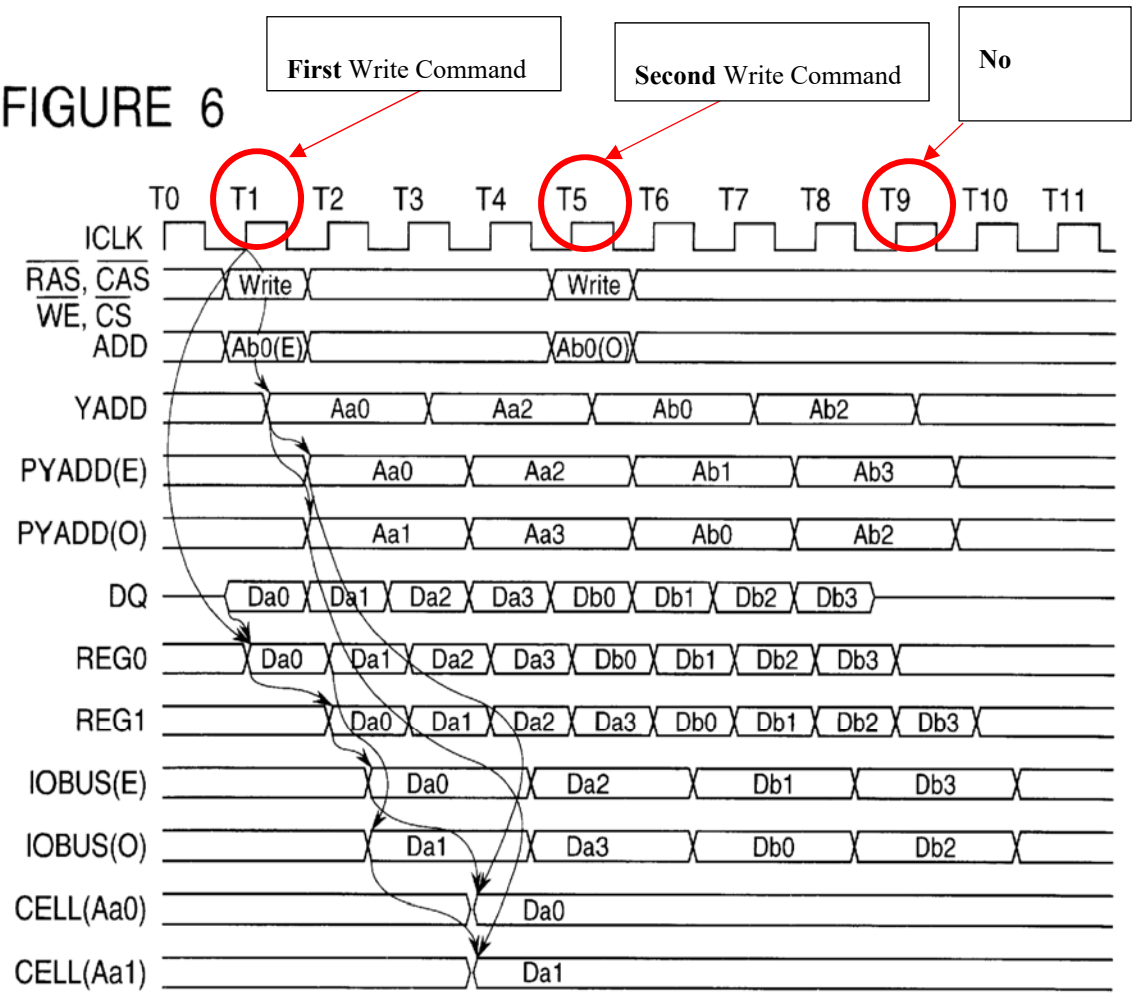
Further, the antecedent basis for a claim term introduced with "said" need not appear in identical words. *Cross Med. Prods. v. Medtronic Sofamor Danek, Inc*., 424 F.3d 1293, 1319 (Fed. Cir. 2005) (holding that "said longitudinal axis of said channel" is not indefinite even though antecedent basis for the longitudinal axis is only implicit in a previously recited "rod"); *Speedtrack, Inc. v.* Wal-*Mart Stores, Inc*., No. C 06-7336 PJH, 2008 U.S. Dist. LEXIS 120644, at *35 (N.D. Cal. June 18, 2008) (finding that "such list" is not indefinite even though antecedent basis for the list uses the different words "category description table.").

Defendants further contend that "said receiving serial data" is indefinite because the word "receiving" could mean a variety of things. Limestone responds that, when read in the context of the context and relevant specification language, "receiving" is clearly a typographical error and should be construed to mean "said ***received*** serial data." In support

of that position, Limestone points out that the specification of the '504 patent it uses the past tense when referring to operating data converted by the input buffer circuit. ('504 patent at 9:39–53).

The Court agrees that "said receiving serial data" should be construed to mean "said received serial data." A POSITA reading the patent specification would recognize that the data transfer cycle has a beginning and an end, and it is indeed a typographical error to assume that the data was continuously received outside the write command cycle.

FIGURE 6



Referring to Fig. 6, a timing diagram based on the present invention shows that the data transfer for a write to memory operation starts with the rising edge of the ICLK at the T1 edge where the write command cycle is initiated. For the case shown in Fig. 6, this first write command cycle ends when the next write command starts at the rising edge of the

ICLK at T5. Fig. 6 shows two consecutive write commands for data transfer cycles, but a POSITA would understand that the received data is transferred to the memory and the memory access continues, if there are additional write requests. Fig 6. shows that it is not required for the data to be transferred continuously, since after the second write command no additional data was transferred. Moreover, claim 1 mentions the initial reference to data in the second limitation: "…internal data buses for inputting and outputting data to and from..," establishing the antecedent for the received data.

For all of these reasons, the Court rules that the phrase "said receiving serial data" means the "external data signals" that the input buffer circuit receives "continuously and sequentially." This result is not only supported by the textual elements discussed above, but is also consistent with one of the basic aims of patent claim construction, which is that "claims should be so construed, if possible, as to sustain their validity." *See e.g., Ruckus Wireless, Inc. v. Innovative Wireless Solution, LLC.*, 824 F.3d 999, 1004 (Fed. Cir. 2016).

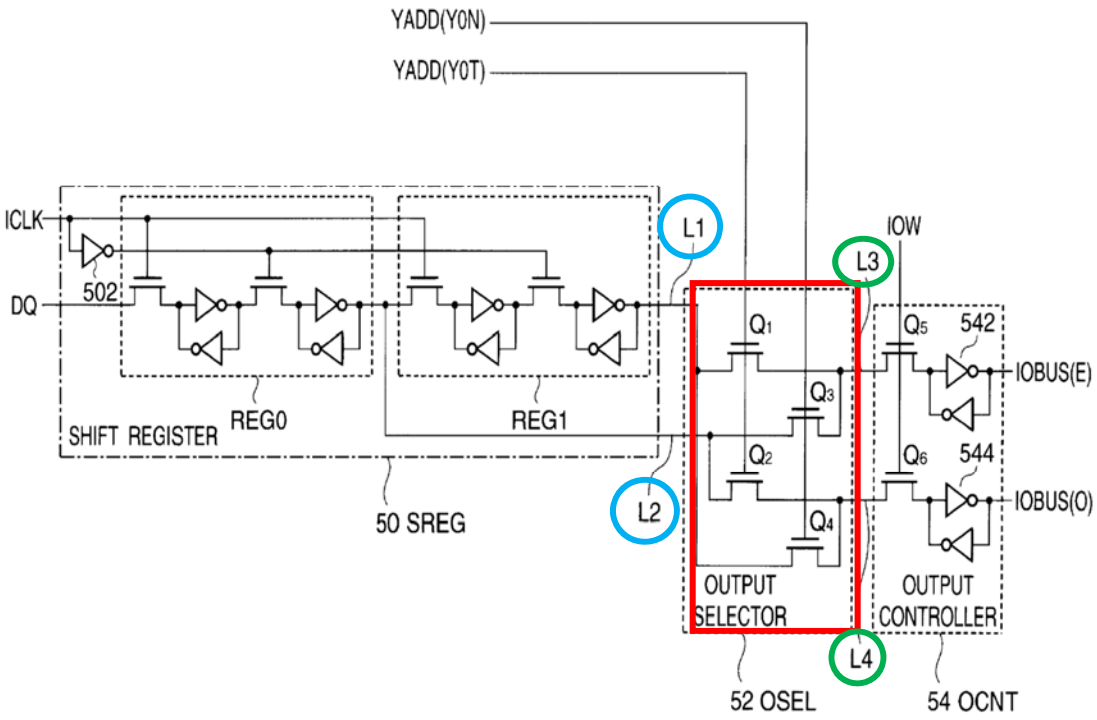
2. Claim 1: "register output selecting means . . ."

Limestone's Construction	Defendants' Construction
This is a means plus function limitation. **Function:** distributing said received parallel data signals, in parallel, to said plurality of internal data buses in accordance with said external address signal **Corresponding structure:** Output Selector 52 of Figure 5, including multiplexers Q1 – Q4 and the external address signals, as described at 9:54–65.	This is a means plus function limitation. **Function:** distributing said received parallel data signals, in parallel, to said plurality of internal data buses in accordance with said external address signal **Corresponding structure:** Output Selector (52) of Figure 5, including multiplexers Q1 – Q4, inputs L1 and L2 and outputs L3 and L4, as described at 9:54–10:17

The parties agree that the "register output selecting means" of claim 1 is a means-plus-function description pursuant to 35 U.S.C. 112, ¶ 6, and that the claimed function is as stated above. The parties disagree on the specifics of the corresponding structure for the output selector 52 of Fig. 5. Specifically, while both sides agree that the multiplexers Q1 to Q4 of output selector 52 of Fig. 5 is structure that corresponds to the claimed "register

output selecting means," the parties disagree as to whether the input L1, L2 and outputs L3, L4 of Fig. 5 should be included in the corresponding structure.

FIGURE 5



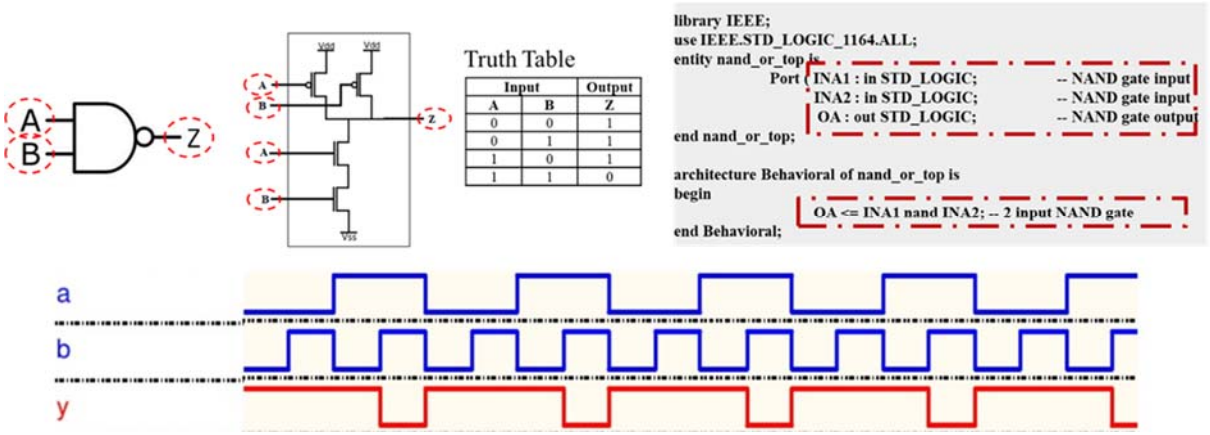
Limestone argues that the transfer gate transistors and not the connections are the structure of the claimed function. These transistors perform the function, and the inputs L1, L2 and outputs L3, L4 do not perform the claimed function.

Defendants argue that the structure, controller (54) of Fig. 5, includes "connections" to buses, because these connections are needed to allow the output control means to perform the claimed function of transferring the parallel data to internal data buses. In particular, Defendants contend that the Q1-Q4 connections allow for distribution of either input to either output line. Thus, the two inputs from L1 and L2 go into output selector 52 and two outputs come out of the output selector through L3 and L4.

However, inputs L1 and L2 are obviously not used to "distribute" the received parallel data signals. The multiplexers perform the distributing function. Moreover, the multiplexers, utilizing the select signals YADD(Y0N) and YADD(Y0T), are all that is

required to perform the claimed function. Specifically, the function of "distributing" is accomplished by the multiplexer outputting one received data or the other based on address signals.

An output selector illustrated as 52 in Fig. 5 has inputs (L1 and L2) and outputs (L3 and L4) that are considered essential parts of the output selector structure. A POSITA familiar with digital circuit design using a hardware description language such as VHDL that is a requirement for a degree in computer engineering understands that in order to design an output selector a design entity must be described. The entity has two parts, each of which is called a design unit when VHDL is used for design and modeling of digital circuits. The entity description represents the external interface of the design, or the input/output designations and the architecture body of the design represents the internal description of the design entity. Therefore, the input and output connections are essential parts of the design.



An example of a NAND gate is shown above where the gate symbolic designation, the detailed transistor description and corresponding inputs and outputs, and the VHDL model are given. In the VHDL description, the input/output designations and the architecture body of the design are highlighted. The design without input/output designations would not be practiced by a POSITA. Accordingly, the subject language is construed to mean that the register output selector 52 of Fig. 5 includes connections L1-L4.

3. Claim 1: "external address signal"

Limestone's Construction	Defendants' Construction
No construction necessary Alternatively, "external address signal" means "a signal used to distribute data signals to internal data buses"	No construction necessary a signal generated outside of the semiconductor memory that uniquely identifies a memory location

Claim 1 recites "a register output selecting means . . . for ***distributing*** said received parallel data signals, in parallel, to said plurality of internal data buses ***in accordance with said external address signal***." ('504 patent at 17:9–14).

According to Limestone, the phrase "external address signal" describes a signal used to distribute data signals to internal data buses, which in turn connect to and from numerous memory locations to store data. Nothing in claim 1 either (1) requires "external" to mean generated outside the semiconductor memory, or (2) requires the external address signal to identify a unique memory location to which the subject data is sent.

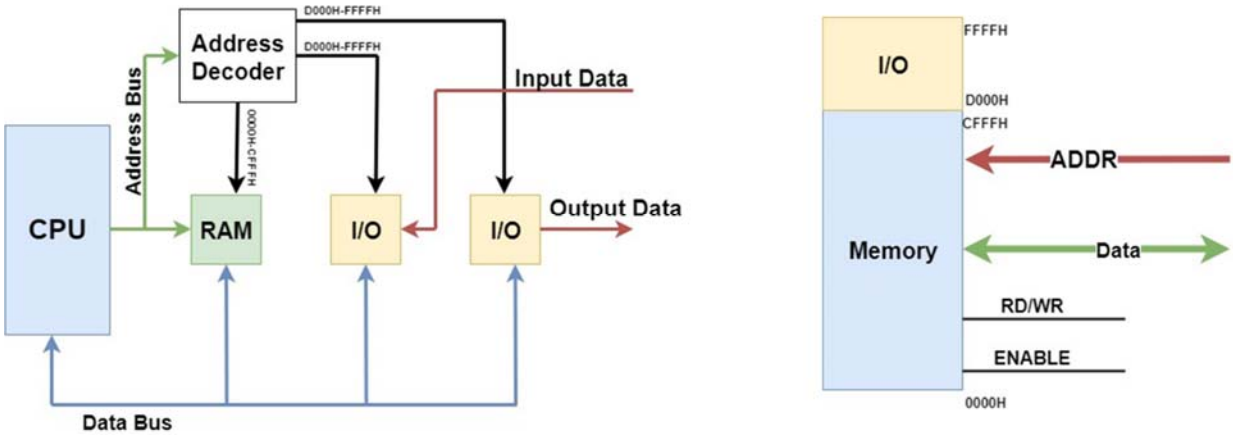
Defendants respond that the phrase "external address signal" has a plain and ordinary meaning and the specification uses the term consistently with this meaning. Defendants also contend that the full external address signal identifies a specific, unique location, citing (but not explaining or even summarizing) a passage from the declaration of its expert, Dr. Pedram.[2]

On the first issue (where the signal is generated), the Court construes the subject language to be a non-technical term that refers to a signal generated outside the semiconductor memory. This signal is designated as ADD in the specification at 3:23-28 with clear reference to an address generated outside the semiconductor device.

On the second issue, the Court concludes that the subject language does not require that particular data be stored only in a unique memory location. In a computer system, the

[2] In its Response Brief, Limestone has objected to Defendants use of long citations to their experts' declarations to provide arguments not specifically made in their briefs, arguing that such a practice constitutes an improper circumvention of briefing page limits. *DeSilva v. DiLeonardi*, 181 F.3d 865, 866-67 (7th Cir. 1999). Incorporation by reference "amounts to a self-help increase in the length of the [] brief." *Id.* "[P]age limits are important to maintain judicial efficiency and ensure fairness to opposing parties." *Corson & Gruman Co. v. N.L.R.B.*, 899 F.2d 47, 50 n.4 (D.C. Cir. 1990).

Central Processing Unit ("CPU") is responsible for processing data by reading instructions and data from the memory and writing the computed results back to the memory. Additionally, the CPU is responsible for reading and writing peripheral devices. These operations include accessing sensors, input/output units, initializing memory devices parameters by writing control registers and reading status registers as well as other peripheral interaction tasks. All these CPU operations occur through different buses that are present in a standard computer system. In almost all the modern CPUs, reading and writing peripheral devices is done be a technique called "memory-mapped-I/O." The accesses for reading and writing peripherals are identical to reading and writing a memory device, the only difference being that certain addresses are set aside for peripherals. As far as the timing and interface signals are concerned, there is no difference.



The above figure illustrates a typical CPU system where the memory (RAM) and I/Os are connected to the address and data bus of the CPU. As far as the CPU is concerned using the memory-mapped-I/O technique there is no difference in reaching RAM or I/O memory locations or registers, respectively. The timing diagram and the CPU instructions for reading and writing are identical. The address decoder shown in the figure will use the I/O address range to activate the I/O devices and those addresses outside that range are destined for memory units.

Therefore, defining the "external address signal" as a signal used to uniquely identify a memory location is unduly narrow and does not cover reading and writing a peripheral device using the "memory-mapped-I/O" technique. A POSITA would not understand the claimed "external address signal" to be limited only to signals that uniquely identify a memory location but, rather, would understand the claimed external address signal broadly to include a signal used to distribute data signals to internal data buses.

Accordingly, the phrase "external address signal," refers to a signal, generated outside the semiconductor memory, used to distribute data signals to internal data buses.

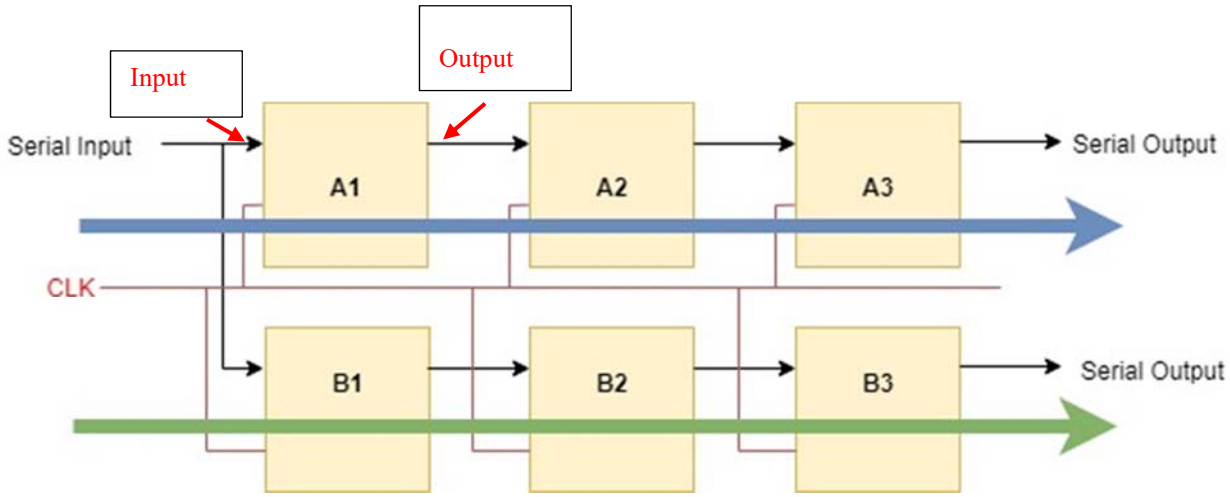
4. Claim 1: "a plurality of cascade-connected registers"

Limestone's Construction	Defendants' Construction
No construction necessary. Alternatively, "a plurality of cascade connected registers" means "two or more registers arranged in series or in a succession of stages so that each subsequent register receives a signal from a preceding register."	No construction necessary. Alternately, "registers arranged in series with the output of each stage connected to the input of the subsequent stage such that as each additional bit is input, it causes the already-input bits to shift through the series of connected registers"

Claim 1 recites an "input buffer circuit" for converting "external data signals" received as "serial data" into "parallel data." The input buffer circuit includes "a shift register circuit composed of a plurality of cascade-connected registers." The cascade-connected registers perform the functions of "latching and shifting said external data signals" and "outputting, in parallel, said data latched in said respective registers."

According to Limestone, the plain language of the claim only requires two or more registers arranged in series or in a succession of stages so that each subsequent register receives a signal from a preceding register. Defendants contend that the subject language requires that the registers be arranged with the output of each stage connected to the input of the subsequent stage, such that as each additional bit is input, it causes the already input bits to shift through the series of connected register.

The notion of cascade-connected registers commonly refers to a series of registers where the output of the first one is connected to the input of the next one and they all are connected to a common clock, creating a shift register used in many digital circuit applications to move bits left or right as well as other related operations. Even if there are two sets of shift registers that are parallel with each other and have the same input and clock signals, a POSITA understands that each one of those shift registers is a set of cascade-connected registers as shown in the figure below.



Registers A1-A3 constitute the first set of cascade-connected register and registers B1-B3 constitute another set of cascade-connected registers. That is all the language of the claim requires.

Accordingly, as Defendants contend, the phrase "a plurality of cascade-connected registers," refers to registers arranged in series with the output of each stage connected to the input of the subsequent stage such that as each additional bit is input, it causes the already-input bits to shift through the series of connected registers.

5. Claims 1 and 2: "reference clock signal"

Limestone's Construction	Defendants' Construction
No construction necessary. Alternatively, a periodic signal used for synchronization	No construction necessary.

	Alternately, a periodic signal with a fixed frequency used for synchronization

Limestone contends that this phrase is not ambiguous. According to Limestone, it means any periodic signal used for synchronization.[3] Defendants, disagree, arguing assertion that the "reference clock signal" has an ordinary and plain meaning that denotes a continuous signal having a fixed frequency.

The Court finds that "clock signal" requires that the signals be transmitted at a fixed frequency or interval. The specification for the '504 patent at 10:43-48 states that the "reference clock CLK" is "supplied with a constant period." The plain meaning of that phrase indicates a fixed frequency or interval.

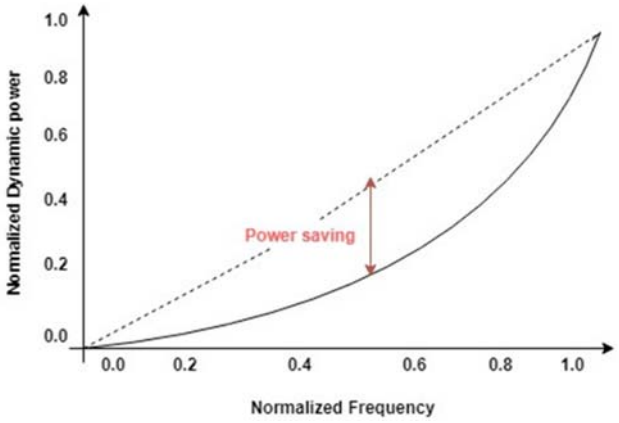
That conclusion is consistent with the operation of a typical synchronous digital circuit. Such a circuit requires a continuously running reference clock that has a fixed frequency used for synchronization throughout the design. A POSITA familiar with low power design understands that a synchronous digital circuit can be designed such that during a low activity condition, the clock frequency can be reduced or completely turned off to lower power consumption. One of the techniques for changing the frequency dynamically is the basis of a well-known technique called Dynamic Voltage Frequency Scaling (DVFS), resulting in many modes of operation with different frequency and voltage values, including when the clock is completely turned off. But as far as the operation of a synchronous digital circuit is concerned, even for a system based on DVFS with different modes of operation, the POSITA understands that the reference clock signal is a fixed continuously toggling synchronization signal used for a given mode of operation.

The figure below shows the overall operation of DVFS and the concept of changing the clock frequency from the maximum designed value (fmax) to zero to achieve lowest dynamic power possible during the idle mode (f = 0). For a given selected mode, the operation frequency is a periodic signal with a fixed frequency.

[3] The parties do not dispute the meaning of the term "reference," which means that the clock signal is a reference for the shift registers to use in latching and shifting external data.

Index	Vdd (volts)	Frequency (MHz)
1	1.2 (V_{max})	2000 (f_{max})
2	1.1	1750
3	1.0	1500
4	0.9	1250
5	0.8	1000 (f_{maxeff})
6	0.8	800
7	0.8	600
8	0.8 (V_{min})	400 (f_{min})
9	NA	0

Idle mode →



Based on the foregoing discussion, the Court construes "reference clock signal" to mean a periodic signal with a fixed frequency that is used for synchronization.

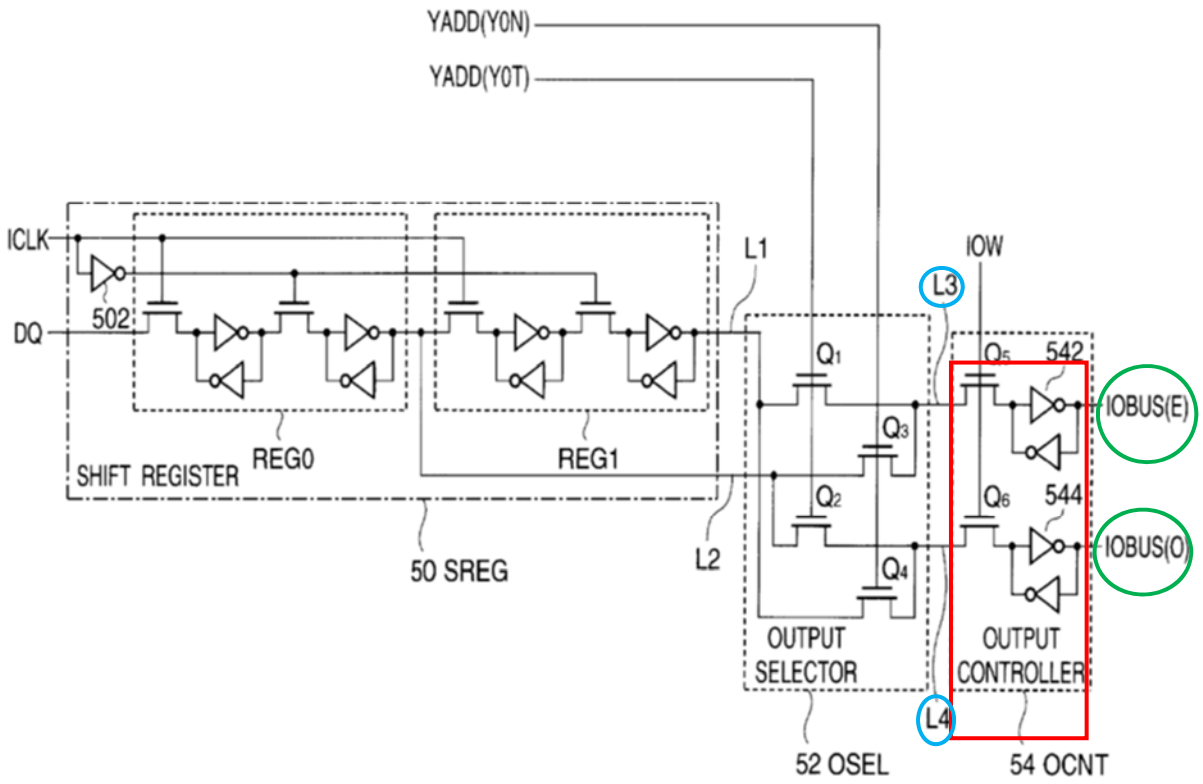
6. Claim 2: "a buffer output control means . . . "

Limestone's Construction	Defendants' Construction
This is a means-plus-function limitation. **Function:** transferring said outputs of said register output selecting means, simultaneously and in parallel, to said plurality of internal data buses, in synchronism with an edge of said reference clock signal by which said external data signal finally supplied to said shift register circuit is latched in said shift register circuit. **Corresponding structure:** Output Controller (54) of Fig. 5 and described at 10:18–33.	This is a means plus function limitation. **Function:** transferring said outputs of said register output selecting means, simultaneously and in parallel, to said plurality of internal data buses, in synchronism with an edge of said reference clock signal by which said external data signal finally supplied to said shift register circuit is latched in said shift register circuit. **Corresponding structure:** Output Controller (54) of Fig. 5 and internal data buses IOBUS(E) and IOBUS(O).

The parties appear to agree on the construction of the subject language. The only potential disagreement involves whether the connections (or "links") to the IOBUS(E) and IOBUS(O) buses comprise part of the corresponding structure needed to allow the output control means to perform the claimed function.

It is not clear from Limestone's briefing whether Limestone disputes that these connections are part of the corresponding structure. Therefore to eliminate any uncertainty, the Court finds that a POSITA understands that the corresponding structure for the output controller (54) of Fig. 5 (shown below) includes the links to input (L3 and L4) and output (IOBUS(E) and IOBUS(O). In fact, the claim describes these connections at 10:18-33.

FIGURE 5



B. The '181 Patent

All semiconductor memory devices, such as DRAMs, inevitably include some number of defective memory cells. To address this problem, DRAM manufacturers have long inserted "redundant" (or "spare") memory cells in their memory devices to replace the defective cells. The '181 Patent uses a specific redundancy scheme that (1) divides a memory into a group of sub-arrays, (2) includes spare cells in only one of the sub-arrays in the group, and (3) allows the spare cells to replace defective cells in any of the sub-arrays

of the group. ('181 Patent, 6:62-67, 16:12-39). Limestone accuses Defendants of infringing claim 3 of the '181 patent (claim 3 depends upon and incorporates the limitations of claims 1-2).

1. Claim 1: "a plurality of first memory blocks . . . the first memory blocks aligned in the column direction"

Limestone's Construction	Defendants' Construction
two or more, but not necessarily all, memory blocks aligned in the column direction	all memory blocks aligned in the column direction

The semiconductor device recited in Claim 1 of the '181 patent has "a plurality of first memory blocks each having a plurality of first normal memory cells" as well as "a plurality of first spare memory cells."

The parties dispute the meaning of the term "plurality." Limestone contends that the ordinary meaning of the word "plurality" is "two or more," citing The Random House Dictionary of the English Language Second Edition (which defines plurality as "a number greater than one") and Federal Circuit authority, including *Dayco Prods., Inc. v. Total Containment, Inc.*, 258 F.3d 1317, 1325-28 (Fed. Cir. 2001) **(**holding that construction of plurality to mean three or more was erroneous as "contrary to its plain meaning" of two or more) (citing *Yorks Prods. Inc. v. Cent. Tractor Farm Family Ctr.*, 99 F.3d 1568, 1575 (Fed. Cir. 1996)); *see also Cybersettle, Inc. v. Nat'l Arbitration Forum, Inc.*, 243 Fed. App'x 603, 606 (Fed. Cir 2007) (unpublished) (noting that "the well understood meaning of the term 'plurality' both in general and in patent parlance" is "two or more").

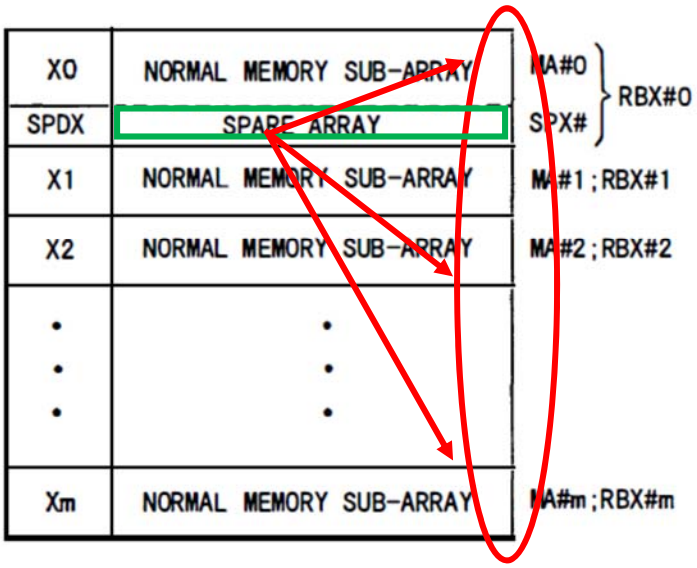
Applying this definition, Limestone asserts that the disputed claim language requires that the semiconductor device have two or more first memory blocks aligned in the column direction. According to Limestone, the inventor deliberately chose the words "*plurality*" and "*first* memory blocks" so that any device having a set of at least two memory blocks aligned in the column direction would satisfy that aspect of the claim.

Defendants disagree. They contend that it is incorrect to focus on the word "plurality" in isolation. While conceding that the "plurality" on its own has been construed

to mean two or more, defendants contend that, when the specification and the file history are considered, the word should be construed to mean "all." In support of that construction, Defendants rely heavily on Fig. 9 in which the spare cell array can replace all the memory blocks, and no additional memory blocks can exist outside these blocks. Furthermore, defendants refer to the file history in which the inventor, allegedly applied Defendants' construction of the term "plurality" and also supposedly disavowed other embodiments besides the one reflected in Figure 9 in order to distinguish prior art and obtain the patent.

Fig. 9 is described as the third embodiment of the invention where the memory array is divided into several row blocks designated as RBX#0 to RBX#m that are formed by the corresponding normal memory arrays MA#0 to MA#m. Among these row blocks, only the first one, RBX#0, has a spare array: SPX#, which is arranged in several rows and sharing the columns with MA#0. SPX# can replace defective normal word lines in normal memory sub-arrays MA#0 to MA#m, which is all the blocks in this embodiment.

FIG. 9



Thus, this embodiment explains its redundancy scheme in the context of replacing defective cells within all of the memory blocks aligned in the column direction, not a subset of these blocks. Defendants urge that the word plurality must be consistent with Fig. 9, because that is the only embodiment that the patentee told the Patent Office ("PTO") that

the '181 Patent covers. Specifically, Defendants argue that (1) the inventor applied Defendants' construction of "first plurality of memory blocks" to distinguish prior art and obtain the patent; and (2) the inventor told the PTO in response to a restriction requirement that claim 1 corresponds to the embodiment of Figure 9. On this basis, Defendants argue that the file history "mandates" that the Court adopt their construction.

"[T]he prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1318 citing *Vitronics*, 90 F.3d at 1582–83. For example, "a patentee may, through a clear and unmistakable disavowal in prosecution history, surrender certain claim scope to which he would otherwise have an exclusive right by virtue of the claim language." *Vita–Mix Corp. v. Basic Holding, Inc.*, 581 F.3d 1317, 1324 (Fed.Cir.2009) (citations omitted). However, "to operate as a disclaimer, [a] statement [by the inventor] in the prosecution history must be clear and unambiguous, and constitute a clear disavowal of scope." *Continental Circuits LLC v. Intel Corporation*, 915 F.3d 788, 798 (Fed. Cir. 2019).

The Court does not believe that the prosecution history rises to this level of clear and unambiguous disavowal. During prosecution, the patentee described prior art ("Lee") as follows: "in Figs. 3A and 3B of Lee, et al., memory cell arrays MCA1 and MCA3 are aligned in the column direction, and memory cell arrays MCA2 and MCA4 are also aligned in the column direction." (10/11/2000 amendment at 5). This does not mean that MCA1, MCA2, MCA3, and MCA4 all have to be included in the *plurality of first* memory blocks aligned in the column direction. The patentee never said that the two columns of blocks are aligned with each other in the column direction, or that they are part of the same plurality. Instead, the patentee addressed the two separate columns of blocks and explained why each column fails to anticipate the shared redundant rows portion of the claim, which was because MCA1 and MCA3 have no redundant cells at all, and MCA2 and MCA4 only have redundant cells that are only associated with those blocks (i.e., RCA1 is associated

with only MCA2 and RCA2 is associated with only MCA4). (10/11/2000 amendment at 5–6).

The patentee further stated that "no redundant memory cell array is provided to the memory cell arrays MCA1 and MCA3." (10/11/2000 amendment at 5–6). There is no mention of sharing memory cell arrays between columns. Accordingly, the patentee was apparently distinguishing Lee by treating the two columns of blocks of Lee separately and addressing both to show that neither column of blocks anticipated the claim. Although this interpretation of the patentee's statements is not beyond dispute, the statements are, at most, ambiguous, and certainly cannot be interpreted as a "clear and unambiguous" disavowal of claim scope. *Continental Circuits*, 915 F.3d at 798.

Defendants' reliance on the prosecution history of the '181 patent is also insufficient to support Defendants' construction of "plurality." Defendants argue that the prosecution history shows that the PTO required the patentee to elect a particular one of seven distinct species (or embodiments), and that the patentee elected "Fig. 9 (claims 4-6[4] being readable thereon) for prosecution." (1/10/00 Election, 1). Defendants argue that this election excludes Fig. 11 as a permissible embodiment of the claim, because the PTO also found that there was no "generic claim" covering multiple species or embodiments.

However, as demonstrated above, the election made by the patentee expressly allowed dependent claims 5 and 6 (corresponding to issued claims 2 and 3). The PTO's prohibition on generic claims covering multiple species must be read to apply to the six *unelected* species, on the one hand – not to the *elected* species and dependent claims based thereon, on the other hand. This makes good sense. Allowing generic claims covering unelected species would, of course, defeat the purpose of the election. By contrast, allowing generic claims covering the species elected by the patentee and dependent species is consistent with the language used by the PTO. The Restriction Requirement specifically indicates that "[u]pon allowance of a generic claim, applicant will be entitled to consideration of claims to *additional species which are written in dependent form*." ('181

[4] Claim 4 corresponds to issued claim 1, and claims 5-6 correspond to issued claims 2-3.

Prosecution History 1/10/00 Office Action at 2) emphasis added). The fact that the PTO contemplated a generic claim necessarily implies that – contrary to Defendants' assertion – some generic claims were permissible, namely, generic claims based on the *elected* species. See also, 37 C.F.R. 1.141(a) ("more than one species of an invention . . . may be specifically claimed . . . provided the application also includes an allowable claim generic to all the claimed species and all the claims to species in excess of one are written in dependent form").

Here, an independent claim (claim 1) was allowed as to the elected species, or embodiment, i.e., Fig. 9. Thus, one can conclude that additional species (Fig. 11 and/or 15) that relate to the claims deemed to be dependent by the PTO (claims 2 and 3) are also allowed. As noted above, that conclusion is consistent with the Restriction Requirement, which explains that an independent claim (such as claim 1) which is generic to dependent claims (such as claims 2 and 3) encompasses the species claimed in those dependent claims. ('181 Prosecution History 1/10/00 Office Action at 2). In short, while the prosecution history is not definitive, it tends to rebuff, rather than support, Defendants' attempt to limit "plurality" to the configuration of memory blocks embodied in Fig. 9.

Given the admittedly ambiguous record, the Court does not agree that the prosecution history "mandates" limiting the scope of the patent in the manner urged by Defendants. As the Federal Circuit has repeatedly cautioned, "because the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Continental Circuits*, 915 F.3d at 796, quoting *Phillips*, 415 F.3d at 1316.

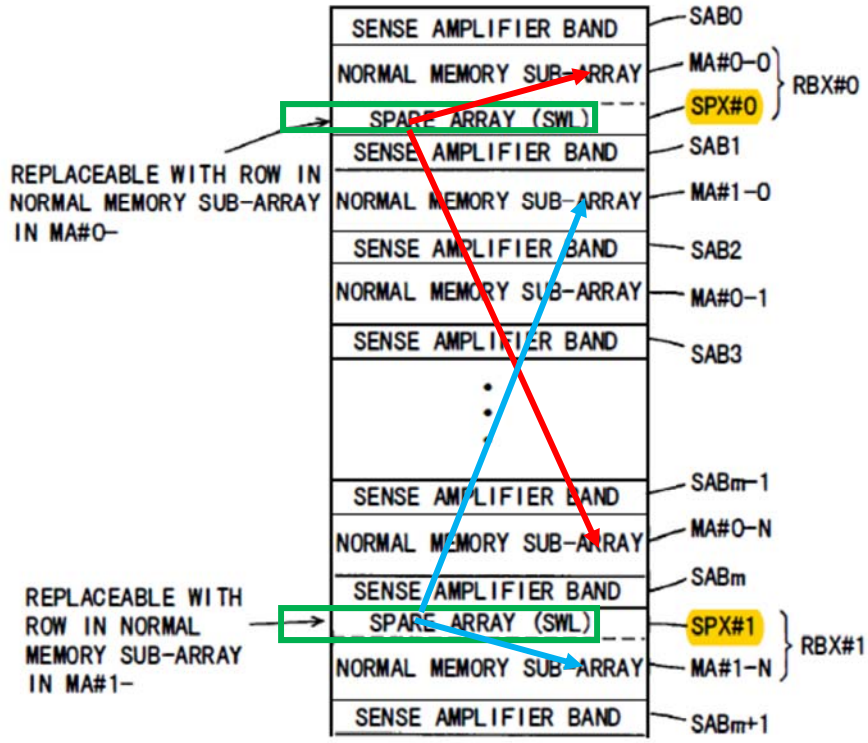
In` the absence of a clear and unambiguous disclaimer by the patentee or any definitive limitation in the prosecution history, the Court must construe the claim language in accordance with the ordinary meaning a POSITA would ascribe to it. Here, the language of the claim does not require that that the "plurality of first memory blocks" aligned in the column direction must include ***all*** memory blocks aligned in the column direction. Nothing

about the language of claim 1 precludes memory blocks other than the plurality of first memory blocks from being arranged in the column direction. Such a construction is inconsistent with the chosen language requiring only a "plurality" of "first" memory blocks, as well as with the transitional phrase "comprising" in the preamble, which allows for the presence of other structures in addition to the specific "first memory block" components specified in the claim. *Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1371 (Fed. Cir. 2005) (claim reciting "comprising . . . a group of first, second, and third blades" encompassed razors having four blades). Accordingly, a POSITA reading the claim as a whole would understand that the word plurality means two or more, including all.

This conclusion is consistent with the specification, which discloses that Fig. 9 is merely one (i.e., the "third") illustrative embodiment intended collectively to illustrate the arrangement of memory blocks. The fourth and fifth embodiments shown in Fig. 11 and Fig. 15, both have a first and second plurality of memory blocks aligned in the column direction.

Specifically, Fig. 11 discloses another embodiment of the invention that shows two distinct memory blocks. The first one is MA#0-0 to MA#0-N and the second one is MA#1-0 to MA#1-N. The specification discloses that SPX0 can replace only the normal word lines in memory sub-arrays MA#0-0 to MA#0-N and SPX1 does the same function only for MA#1-0 to MA#1-N. The specification for this embodiment does not constitute that a spare array can replace all the memory cells, it can only replace the ones belonging to a specific group of memory blocks.

FIG. 11



Based on the language of the claim and specification, including Fig. 11, the Court construes "a plurality of first memory blocks" to mean "two or more memory blocks aligned in the column direction."

2. Claims 1 and 2: "each row of said plurality of first [second] spare memory cells being capable of replacing a defective row including a defective first normal memory cell in said plurality of first [second] memory blocks"

Limestone's Construction	Defendants' Construction
(1) No construction necessary (2) No construction necessary	(1) "in said plurality of first memory blocks" means "in all of the memory blocks aligned in the column direction." (2) "each row . . . being capable of replacing a defective row . . . in said plurality of second memory blocks" means "each row is capable of replacing a defective row. . . anywhere in the second plurality of memory blocks but

	not in any other plurality of memory blocks."

Limestone asserts that the subject language is not ambiguous and requires no construction. Defendants bring forward two disputes. First, Defendants argue that construction is necessary to "clarify" that each row of the plurality of first spare memory cells must be capable of replacing a defective row anywhere in the plurality of first memory blocks – i.e., in all of the memory blocks aligned in the column direction. Second, Defendants argue that the first spare cells cannot be used to replace defective rows in the second blocks, and the second spare cells cannot be used to replace defective rows in the first block.

The Court does not believe that Defendants' proposed constructions clarify any legitimate ambiguity, but import extraneous limitations into claims 1 and 2. Defendants' construction would require that each row of first spare memory cells be capable of replacing ***any*** defective row in the plurality of first memory blocks. In other words, they contend that a row of first spare memory cells capable of replacing some, but not all, defective rows of a first plurality of memory blocks does not fall within the claim. But claim 1 contains no such requirement. The plain language of claim 1 only requires "each row of said plurality of first spare memory cells being capable of replacing ***a*** defective row including a defective first normal memory cell in said plurality of first memory blocks." Defendants' construction treats the claim as if "capable of replacing ***a*** defective row" read "capable of replacing ***all*** defective ***rows***" of the first memory blocks. The Court concludes that the word "a" should be given its plain meaning and not construed to mean "all."

Second, Defendants' construction would require that one plurality of memory blocks be capable of replacing defective rows only in the same plurality of blocks. However, the claim language requiring that "the first spare memory cells" be "capable of replacing a defective row including a defective first normal memory cell in said plurality of first memory blocks" does not impose a restriction whereby first spare memory can ***only*** replace a defective row located in the plurality of first memory blocks. The Court finds

that the plain language does not exclude devices in which "first spare memory cells" are also capable of replacing defective cells in a plurality of second memory blocks.

3. Claim 2: "a plurality of second memory blocks arranged alternatively with said plurality of first memory blocks along the column direction"

Limestone's Construction	Defendants' Construction
No construction necessary, not indefinite	Indefinite

Using their definition of "plurality" discussed in Section 1, above, Defendants argue that the subject language is indefinite. According to defendants, because "plurality of first memory blocks" includes ***all*** blocks aligned in the column direction, there cannot be other blocks (i.e., a plurality of second memory blocks) aligned in the same direction.

This construction would make it impossible for the semiconductor device to have the "plurality of second memory blocks" recited in dependent claim 2 and referenced in other dependent claims. In other words, it renders certain terms of claim language meaningless, and is therefore untenable. *Wasica Fin. GmbH v. Continental Auto. Sys., Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017); ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous"); *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 - 51 (Fed. Cir. 2006) (refusing to construe claim terms in a way that made other limitations meaningless). The Court declines to adopt Defendants' construction.

As set forth above, the Court has concluded that "plurality" means two or more memory blocks – not all memory blocks. Using this construction, the meaning of the phrase "plurality of second memory blocks" in claim 2 is not indefinite or meaningless; rather it acts to impose an additional requirement that is easily understandable to a POSITA. Accordingly, the Court concludes that the subject language is not ambiguous, and refers to the alignment of some (but not necessarily all) of second memory blocks in the same column direction.

4. Claims 1 and 2: "a plurality of first [second] spare memory cells arranged in a matrix of rows and columns in a particular one of said plurality of first [second] memory blocks"[5]

Limestone's Construction	Defendants' Construction
No construction necessary, but if the Court finds it necessary to construe the term, it means "two or more, but not necessarily all, memory blocks aligned in the column direction."	Indefinite. Alternately, the claim requires that only one of the "plurality of first [second] memory blocks" can contain spare memory cells.

As set forth in its Response Brief, Limestone agrees with Defendants that the subject language means that the first [second] spare memory cells cannot be divided among a plurality of memory blocks. According to Limestone, this does not preclude the existence of additional spare memory cells, such as third spare memory cells, in one of the plurality of first [second] memory blocks other than the "particular one" referenced in the claim language.

Defendants assert that the plain meaning of the phrase "in a particular one" requires that the spare cells be in only one, and not more than one, block of each plurality of memory blocks.

The Court agrees that the meaning of the phrase "in a particular one" is a non-technical term that should be construed according to its ordinary, commonly understood meaning: "a single one." *See, e.g.* Webster's Encyclopedic Unabridged Dictionary at 1415 (defining "particular" to mean "of or pertaining to a single or specific, person, thing, group, class, occasion, etc., rather than to others or all."); *see also Broadcast Innovation LLC v. Echostar Commc'ns. Corp.*, 240 F. Supp. 2d 1127, 1152 (D. Colo. 2003) (construing the phrase "a particular one" and finding no meaningful difference between a construction of "one and only one" and no construction at all: "One is in the singular and means one, whether it is 'a particular one' or 'one and only one'"). Indeed, both parties' experts appear to agree with this ordinary meaning. Pedram Decl. ¶ 157 ("A person of ordinary skill in

[5] Claims 1 and 2 contain parallel claim limitations as indicated by the bracketed portion of the term. Accordingly, the construction of the limitation in claim 2 applies equally to this limitation in claim 1.

the art would have understood the phrase 'a particular one' to be consistent with its plain meaning—a single one."); Rhyne Tr., 69:20-22 ("Q. What does 'particular' mean to you? A. It means it's one – it's a block.") (objections omitted).

The Federal Circuit also has held that "particular" refers to a single one. In *Wisconsin Alumni Research Foundation v. Apple Inc.*, the Federal Circuit reversed the denial of a motion for judgment as a matter of law of no infringement and determined that none of the accused products practiced the limitation of "[a/the] ***particular*** [load] instruction." 905 F.3d 1341, 1346-47 (Fed. Cir. 2018) (emphasis added). In the Federal Circuit's opinion, the plain meaning of "particular" in view of the patent required association with a ***single*** load instruction, ***not*** association with ***multiple*** load instructions. *Id.* at 1348 ("In our view, the plain meaning of 'particular,' as understood by a person of ordinary skill in the art after reading the [asserted] patent, requires the prediction to be associated with ***a single load instruction. A prediction that is associated with more than one load instruction does not meet this limitation***") (underlined emphasis original).

This plain and ordinary meaning is consistent with the '181 patent's claim language, specification, and prosecution history. Claims 1 and 2 require that the "plurality of first [or second] spare memory cells" be "in a particular one of said plurality of first [or second] memory blocks." They do not state that those "spare memory cells" are in "a block," in "at least one block," or just "in said blocks." Instead, they specifically require the spare cells to be "in a particular one" of the blocks. Interpretation of claims 1 and 2 in a manner that permits the spare memory cells for each plurality to be in more than one block would ignore this explicit language and effectively read the word "particular" out of the claims. *See Felix v. Am. Honda Motor Co.*, 562 F.3d 1167, 1178 (Fed. Cir. 2009) (rejecting proposed construction of term "mounted" that would render adverb "pivotally" meaningless). If the patentee wanted to claim a system in which spare cells for a plurality could be spread throughout more than one block, he could have simply claimed, for example, "a plurality of first [second] spare memory cells arranged in a matrix of rows and columns in ~~*a particular one of*~~ said plurality of first [second] memory blocks." He did not.

The specification further confirms that the patentee viewed his invention as one wherein the spare cells for each plurality of memory blocks are contained in just one block of the plurality. *See Abbott Labs. v. Sandoz, Inc*., 566 F.3d 1282, 1288 (Fed. Cir. 2009) ("[C]laims cannot enlarge what is patented beyond what the inventor has described as the invention.") (citation omitted). Indeed, the '181 patent confirms that this feature is the invention: "in a semiconductor memory device ***according to the present invention***, spare lines are provided ***together as a single array***, [and] a plurality of memory mats are provided corresponding to the spare arrays." ('181 Patent, 6:62-67) (emphasis added). Such statements, which relate to features of the "present invention," serve to limit and define the scope of the claims. *See, e.g.*, *Verizon Servs Corp. v. Vonage Holdings Corp.*., 503 F.3d 1295, 1308 (Fed. Cir. 2007). Thus, even if the claims did not already make clear that all the spare cells must be located in one block, the specification emphasizes that this is a feature of the "present invention."

The Court concludes that the phrase "in a particular one" requires that the spare cells be in only one, and not more than one, block of each plurality of memory blocks.

C. The '296 Patent

The '296 patent relates to activating and deactivating input buffers in semiconductor devices. When a signal is input to a semiconductor device, the device typically contains an input buffer to drive the signal through the chip. In the active state, the buffer allows the input signal to pass through to the output. In the inactive state, the buffer blocks the signal passage. A buffer may also have an enable input that activates and deactivates the buffer. To reduce power consumption, a semiconductor device may have low power modes in which internal signals, and their corresponding input buffers, are disabled.

Limestone accuses Defendants of infringing independent apparatus claim 13 and its dependent claims 14 and 15.

1. Claim 13: "a signal specifying whether control on said signal input circuitry by an operation activation signal is valid"

Limestone's Construction	Defendants' Construction
No construction necessary.	"a signal that is independent from the operation activation signal and that determines whether the operation activation signal may be used to activate and deactivate the signal input circuitry."

Defendants believe that claims construction is necessary to make explicit a concept which supposedly underlies the claims language. Specifically, Defendants seek to construe the relevant language as describing "a signal that is ***independent from*** the operation activation signal and that determines whether the operation activation signal may be used to ***activate and deactivate the signal input circuitry***."

Limestone responds that no construction is necessary. Claim 13 already separately recites (1) an operation activation signal ("Activation Signal") and (2) a signal specifying whether that activation signal is valid ("Validation Signal"). There is no technical basis for arguing that these signals must be independent. Adding the requirement that these signals be independent creates ambiguity where there was none.

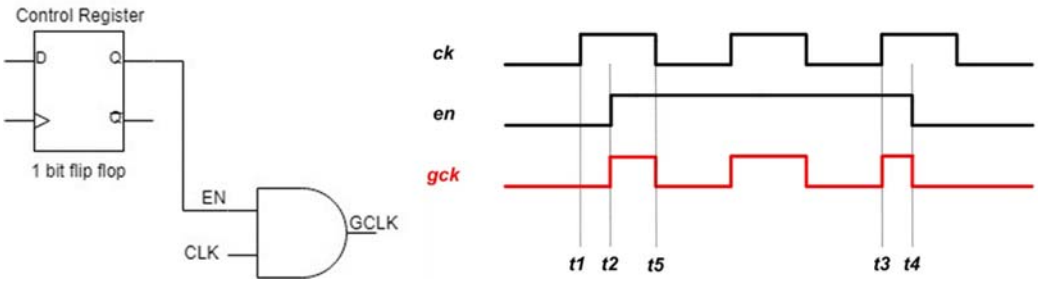
Claim 13 recites, in part, "register circuitry for storing a signal specifying whether control on said signal input circuitry by an operation activation signal is valid, said operation activating signal indicating whether an external signal is a valid signal." The latter portions of the claim further describe the output of the activation control circuit, determined based on the state of the respective signals. The claim does not require the signals to be "independent" or say anything about how the signals may or may not relate to other signals. Moreover, both signals are part of the claimed mechanism for activating and deactivating the signal input circuitry, and thus the concept of "independent from" is directly contrary to the claim. A POSITA readily understands from the claim language that it is not necessary to declare that the Activation Signal is independent from the Validation Signal, because this disclosure does not impact the teaching of the invention.

The plain and ordinary understanding of the patent does not require any relationship between these two signals.

Further, the meaning of "valid" in the disputed claim phrase is apparent from claim 13 as a whole. According to the claim, when the stored signal in the register circuitry indicates that control of activation and deactivation by the operation activation signal is "valid," the "activation control circuit selectively activates said signal input circuitry according to said operation activation signal." When the stored signal indicates that control on the signal input circuitry by the operation activation signal is "invalid," the activation control circuit responds by "holding said signal input circuitry in an active state." ('296 Claim, 28:37-38)

The specification also supports the conclusion that the two signals work in concert – not independently. The embodiment illustrated in Figs. 17–20 of the '296 patent describes a CKE reset circuit 62 including a register (62e) that stores a signal used to specify whether control on signal input circuitry by an operation activation signal is valid, i.e., the Validation Signal.

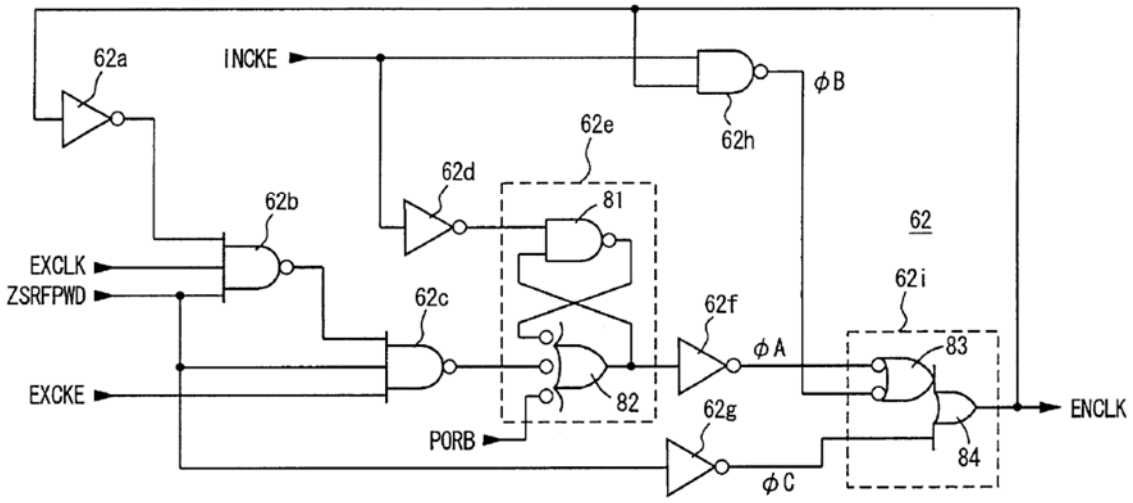
In logic design generally, "validation" is equivalent to enabling or qualifying a signal (in common parlance, turning it on and off). For instance, a clock signal can be turned off by a simple technique called clock gating where the clock is turned off when the control signal is disabled (invalidated), as shown by the simple example of a clock below:



The control register in the above example receives and stores the Validation Signal.

The register 62e in Fig. 20 performs the same function; it receives and stores the Validation Signal, which can be changed by an external instruction.

FIG. 20



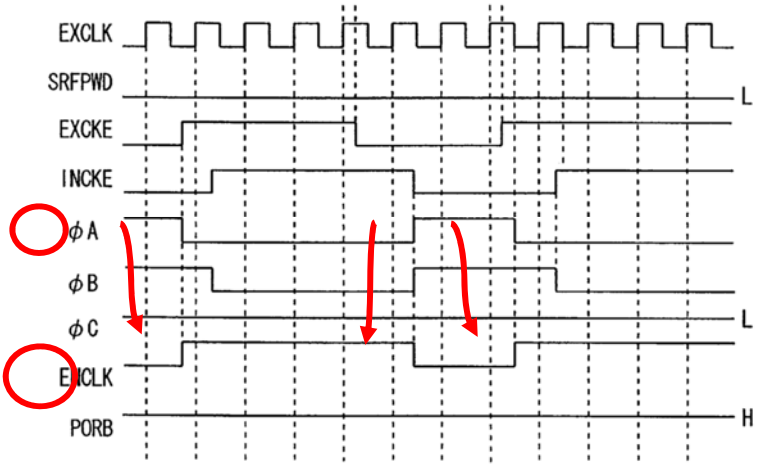
One of the main differences between the simple register in the first example and the register (62e) referenced in Fig. 20 is that the latter is an R/S[6] flip flop registers with many inputs controlling its stored data. Another difference is that the output that generates the EN (or ENCLK) signal is a simple wire, whereas, in Fig. 20, there are multiple connections and logical gates that collectively generate the Activation Signal.

In this sense, the Validation Signal and Activation Signal work in tandem and can be deemed related or "interdependent." Accordingly, it would do violence to the claim language to insert the adjective "independent" to describe the two signals.

Fig. 21 shows the relationship between the Validation Signal (represented by φ A) and the output of the control register (62e), which is the Activation Signal (represented by ENCLK).

[6] "R/S" means reset/ set.

FIG. 21



For the foregoing reasons, the Court construes "[register circuitry for storing] a signal specifying whether control on said signal input circuitry by an operation activation signal is valid" to mean a signal that is merely distinct – not independent – from the operation activation signal that determines whether the operation activation signal may be used to activate and deactivate the signal input circuity.

2. Claim 13: "an activation control circuit . . . "

Limestone's Construction	Defendants' Construction
This is not a means-plus-function limitation. If the Court finds otherwise, then the corresponding structure is the composite gate 62i illustrated in Fig. 20 and described at 23:33–41.	This is a means-plus-function limitation. **Corresponding Structure**: Indefinite – no corresponding structure.

The parties dispute whether the claims language operates as a means-plus-function description pursuant to 35 U.S.C. 112, ¶ 6. According to Defendants, the subject language recites generic terms that provide no structure ("activation control circuit") to perform functions, namely, "selectively activating said signal input circuitry" and "holding said signal input circuitry in an active state all the times." Defendants further contend that the '296 specification fails to describe any structure that performs these functions, claim 13 and the claims that depend on it are indefinite.

Limestone contends that the subject language does not rely on a means-plus-function description, because it references an "activation control circuit" that performs certain logical operations, including receiving the Activation Signal and Validation Signal. According to Limestone, a POSITA would recognize a limited selection of structures capable of performing the described functions.

The Court finds that Limestone fails to identify sufficient structure in the claims to avoid the application of Section 112, ¶ 6. The Federal Circuit has expressly declined to hold that the term "circuit" is sufficient to avoid application of Section 112, ¶ 6. *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1373 (Fed. Cir. 2003) ("[W]e do not find it necessary to hold that the term 'circuit' by itself always connotes sufficient structure"). More recently, in *Williamson v. Citrix Online, LLC*, the Federal Circuit held that for a claim limitation expressed in functional language without using the word "means," the presumption against application of Section 112, ¶ 6 can be overcome without showing that the limitation is "essentially [] devoid of anything that can be construed as structure." 792 F.3d 1339, 1349 (Fed. Cir. 2015). Thus, the *Williamson* test does not require an absolute lack of structure to invoke Section 112, ¶ 6. *Id.* The presumption is overcome when the challenger establishes by a preponderance of the evidence that "the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function." *Zeroclick LLC v. Apple, Inc.*, 891 F.3d 1003, 1007 (Fed. Cir. 2018) (quoting *Williamson*, 792 F.3d at 1349) (internal quotations omitted).

Applying *Williamson*, courts have analyzed "circuit" claim terms on a case-by-case basis to determine whether the term fails to recite sufficiently definite structure that performs the claimed function. *See Koninklijke Philips N.V. v. ZOLL Lifecor Corp.*, No. 2:12-CV-1369, 2015 WL 12781199, at *14 (W.D. Pa. Aug. 28, 2015) (holding that claim term "a connecting mechanism forming an electrical circuit with the energy source and the electrodes when the electrodes are attached to a patient" was a means-plus-function limitation because "[t]he term 'circuit' here is plainly being used here in its generic sense as 'the complete path of an electric current including usually the source of electric energy.'

http://www.merriamwebster.com/dictionary/circuit."); *see also Williamson*, 792 F.3d at 1349.

Defendants have submitted evidence (which Limestone does not dispute) that, in the context of the '296 patent, the plain and ordinary meaning of the word "circuit" is a "combination of electrical components interconnected to perform a particular task." (8/27/19 Pedram Decl. ¶ 99). These components perform logical operations – but the reference to logical operations in the disputed term does not limit the selection of components that may perform such logical operations. (*Id*., ¶¶ 100-102). Indeed, Limestone's own expert, Dr. Khatri concedes that in this context, "it is well-known in the art that different logic gates and signal polarities can be used interchangeably to achieve the same result." (Khatri Infringement Report, ¶ 123). For a given logic function, an infinite number of different logic gate combinations may perform the function. (8/27/19 Pedram Decl. ¶ 101.)

The claim language reciting the functions of the "activation control circuit," which Limestone characterizes as "logical relationships" between claim elements, says nothing about the structure of the circuit. *MTD Products Inc. v. Iancu* 2019 WL 3770828 (Fed. Cir. Aug. 12, 2019). There, the Federal Circuit held that "mechanical control assembly" is a means-plus-function limitation even though the claim described that the "mechanical control assembly" is "coupled to the left and right drive units" and described functions of the assembly in logical terms:

> the mechanical control assembly being configured such that ***if the speed control member is shifted from*** (a) a forward position in which the left drive wheel is rotating in a forward direction at a first forward speed and the right drive wheel is rotating in a forward direction at a second forward speed that is ***less than*** the first forward speed as a result of the steering device being in a first right turn position ***to*** (b) a reverse position ***while*** the first right turn position of the steering device is maintained, ***then the left drive wheel will rotate in a reverse direction***

at a first reverse speed ***and the right drive wheel will rotate in a reverse direction*** at a second reverse speed that is less than the first reverse speed.

Id., at *5-7 (Fed. Cir. Aug. 12, 2019).

Thus, logical, functional descriptions of a claim limitation are not a substitute for corresponding structure. Here, a POSITA would not understand the term "activation control circuit" and the remaining claim language to provide "a sufficiently definite meaning as the name for structure." *Williamson*, 792 F.3d at 1349. The claim merely recites functions of activating, deactivating, and holding an input buffer active. Nothing suggests what types of logic circuits are used implement these functions. Thus, because the specification does not disclose the corresponding structure to perform the claimed functions, Section 112, ¶ 6 applies.

Anticipating that this might be the case, Limestone asserts as a fallback position that, if the subject language is construed as a means-plus-function claim, then the corresponding structure is the composite gate 62i illustrated in Fig. 20 and described at 23:33-41 of the '296 patent. However, neither in its Opening Brief nor in its Response does Limestone demonstrate in what manner Fig. 20 is the corresponding structure for the "activation control circuit." Instead, Limestone directs the Court, without explanation, to review Paragraphs 64-66 of the declaration of its expert, Dr. Khatri. As Defendants point out, Dr. Khatri uses a modified version of Fig. 20 that differs in several material respects from the Fig. 20 illustrated in the specification. Hence that extrinsic evidence is entitled to no weight. An expert's statements cannot be used to "rewrite the patent's specification" to provide corresponding structure for a means-plus-function limitation. *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1332 (Fed. Cir. 2003); *see also Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584 (Fed. Cir. 1995) (extrinsic evidence may not be used to contradict the specification).

In conclusion, the Court construes the subject language as a means-plus-function claim pursuant to 35 U.S.C. 112, ¶ 6. Given the absence of any corresponding structure necessary to satisfy that provision, the Court concludes that Defendants have shown by

clear and convincing evidence that the claim is indefinite. The entire limitation after "for" in this claim fails to teach a POSITA the necessary structure for the invention.

IV. Disposition

For the reasons stated above, the Court construes the disputed terms as follows:

Dated: September 11, 2019

DAVID O. CARTER
U.S. District Judge

'504 Patent

- Claim 1: "said receiving serial data" means the "external data signals" that the input buffer circuit receives "continuously and sequentially."
- Claim 1: "register output selecting means . . ." is a means-plus-function limitation and the Court finds the corresponding structure register output selector 52 of Fig. 5 includes connections L1-L4.
- Claim 1: "external address signal" means a signal, generated outside the semiconductor memory, used to distribute data signals to internal data buses.
- Claim 1: "a plurality of cascade-connected registers" refers to registers arranged in series with the output of each stage connected to the input of the subsequent stage such that as each additional bit is input, it causes the already-input bits to shift through the series of connected registers.
- Claims 1 and 2: "reference clock signal" means a periodic signal with a fixed frequency that is used for synchronization.
- Claim 2: "a buffer output control means . . . " is a means-plus-function limitation and the Court finds the corresponding structure for the output controller (54) of Fig. 5 includes the links to input (L3 and L4) and output (IOBUS(E) and IOBUS(O)).

'181 Patent

- Claim 1: "a plurality of first memory blocks . . . the first memory blocks aligned in the column direction" means "two or more memory blocks aligned in the column direction."
- Claims 1 and 2: "each row of said plurality of first [second] spare memory cells being capable of replacing a defective row including a defective first normal memory cell in said plurality of first [second] memory block." The Court concludes that the word "a" should be given its plain meaning and not construed to mean "all." The Court further

concludes that Defendants' proposed restriction whereby first spare memory can only replace a defective row located in the plurality of first memory blocks is incorrect.

- Claim 2: "a plurality of second memory blocks arranged alternatively with said plurality of first memory blocks along the column direction" is not indefinite or meaningless. The Court concludes that the language refers to the alignment of some (but not necessarily all) of second memory blocks in the same column direction.
- Claims 1 and 2: "a plurality of first [second] spare memory cells arranged in a matrix of rows and columns in a particular one of said plurality of first [second] memory blocks" requires that the spare cells be in only one, and not more than one, block of each plurality of memory blocks.

'296 Patent

- Claim 13: "a signal specifying whether control on said signal input circuitry by an operation activation signal is valid" means a signal that is merely distinct – not independent – from the operation activation signal that determines whether the operation activation signal may be used to activate and deactivate the signal input circuity.
- Claim 13: "an activation control circuit . . . " is a means-plus-function limitation with no corresponding structure. The Court finds this claim is indefinite.